JC17 Rec'd PCT/PTO 21 JUN 2001

*FORM PTO 1390 (REV 11-2000)

U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER: 449122006400

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

U.S APPLICATION NO. (If known, see 37 CFR 1 5): 09/868773 Not yet assigned

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE99/03881	30 November 1999	23 December 1998

TITLE OF INVENTION: **METHOD FOR SYNCHRONIZING SEVERAL DIGITAL INPUT SIGNALS**

APPLICANT(S) FOR DO/EO/US: **Andreas JURISCH**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

☒ An English language translation of the International Application under PCT Article 19 (35 U S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).

☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made, however, the time limit for making such amendments has NOT expired
   d. ☐ have not been made and will not be made.

☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C 371(c)(3)).

☒ An oath or declaration of the inventor(s) (35 U S C. 371(c)(4)).

10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U S C 371(c)(5))

Items 11. to 16. below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4)
19. ☐ A second copy of the English language translation of the international application under 35 U S.C. 154(d)(4).
20. ☒ Other items or information: 1. International Search Report 2. IPER 3. Information Data Sheet 4. Return receipt postcard

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on June 21, 2001

Marieta Luke

dc-268009

JC16 Rec'd PCT/PTO 21 JUN 2001

U.S. APPLICATION NO (if known, see 37 CFR 1.5) Not yet assigned 09/868773	INTERNATIONAL APPLICATION NO. PCT/DE99/03881	ATTORNEY'S DOCKET NUMBER 449122006400

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO.....$1,000.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO.....$860.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO.....$710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provision of PCT Article 33(1)-(4) $690.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

CALCULATIONS PTO USE ONLY

ENTER APPROPRIATE BASIC FEE AMOUNT =				$860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$0	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	6 - 20 =	0	x $18.00	$0	
Independent claims	1 - 3 =	0	x $80.00	$0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$270.00	
TOTAL OF ABOVE CALCULATIONS =				$1130.00	
Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.				$0	
SUBTOTAL =				$1130.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$0	
TOTAL NATIONAL FEE =				$1130.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00 per property** +				$40.00	
TOTAL FEES ENCLOSED =				$1170.00	
				Amount to be refunded:	**$**
				charged:	**$**

a. ☒ A check in the amount of $1,170.00 to cover the above fees is enclosed.

b. ☒ The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment to **Deposit Account No. 03-1952**.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kevin R. Spivak
Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888

Kevin R. Spivak
SIGNATURE

Kevin R. Spivak
Registration No. 43,148

Description

Method for synchronizing a plurality of digital input signals

The invention relates to a method for synchronizing a plurality of digital input signals which are formed by sampling with the aid of a dedicated operating clock in each case.

A method of this type can be gathered from the European patent specification EP 0 198 684 B1. According to this method, specifically, a differential relay described in this patent specification operates to protect an electric power transmission line which is monitored at various points with regard to the current flowing through. The currents at the various points on the power transmission line are converted into digital input signals by using a dedicated operating clock in each case to sample the power supply line to be monitored at the various points; the sampling is undertaken in this case at the various points not with the aid of a synchronous clock, but with the aid of weakly differing clock frequencies. Running between the various points of the power supply line is a digital transmission channel via which a calling message is transmitted by a detecting device (master) at one point of the power supply line to another point, the calling message also including data which give information on the sampling instant at the one point. In response to the calling message, a detecting device (slave) at the other point of the power supply line emits a return signal which includes, inter alia, the information on the sampling instant in the master and on a time difference between the last sampling instant in the slave

and the subsequent receiving instant of the calling message in the slave. The return signal received by the master is used in the master to draw a conclusion on the temporal skew of the sampling instants at the two different points on the power supply line, and the time skew is compensated with regard to the various sampling instants after a vector transformation of the received data by means of an appropriate pointer rotation.

It is the object of the invention to develop a method for synchronizing a plurality of digital input signals such that it can be carried out relatively easily and reliably without the need to form pointer variables.

According to the invention, in order to achieve this object in the case of a method of the type specified at the beginning, digital auxiliary signals are formed by sampling the digital input signals with the aid of a common postprocessing clock, use being made of a postprocessing clock which is at least twice as fast as the slowest operating clock; synchronized digital output signals which correspond to the digital input signals are formed by means of interpolating each digital auxiliary signal.

A substantial advantage of the method according to the invention consists in that it can be used to synchronize a plurality of digital input signals even when these input signals are formed from analog input signals by sampling with the aid in each case of a very different operating clock. Consequently, the clock generators required for generating the operating clocks need to fulfil only relatively low requirements for the purpose of carrying out the method according to the invention. Moreover,

the method according to the invention places relatively modest requirements on the quality of the transmission channels. A further important advantage consists in that the method according to the invention can be carried out relatively easily, because the sampling of digital input signals with the aid of a common postprocessing clock, and the interpolation of the digital auxiliary variables thus formed are well-established measures per se.

The method according to the invention can be carried out with sufficient accuracy whenever the digital input variables are sinusoidal and/or cosinusoidal signals. This is frequently not the case, and so it is necessary then to accept relatively large errors. If this is not acceptable with regard to the given requirements, it seems to be advantageous in accordance with a development of the invention when, before being sampled with the aid of the common postprocessing clock, the digital input signals are filtered with the aid of a filter having a characteristic which is the inverse of the characteristic of an interpolation filter used for the interpolation. In this embodiment of the method according to the invention, a transmission characteristic with the value 1 results on the transmission link of the digital input variables up to the formation of the digital output variables, resulting in the possibility of forming digital output variables which correspond very perfectly to the digital input variables.

It has proved to be advantageous in the case of the method according to the invention when filtering with the aid of an antialiasing filter is undertaken directly after the interpolation, in order to achieve a bandwidth limitation for an evaluation device to which the digital output signals are to be applied.

The digital input signals to be synchronized can be of very different formation. For example, they can be output signals of sensors which respectively use individual clock generators to output digital signals at their output from analog input variables. Furthermore, the digital input signals can be generated from analog measured variables of an electric power supply system by sampling at various points on the power supply system. The method according to the invention is to be regarded as particularly advantageous when the digital input variables are obtained from secondary variables, sampled with the aid in each case of a dedicated operating clock, of measuring transducers in an electric power supply system. In this case, the measuring transducers can be arranged at various positions, for example in a transformer substation, or can be obtained as a component of a differential protective arrangement at the ends of an electric power supply line or at other terminals of a generator or power transformer.

If the measuring transducers are Rogovsky measuring transducers, the digital input signals formed from the secondary variables of such measuring transducers are converted directly into the digital auxiliary variables, and an integrator is used for the interpolation.

For the purpose of further explaining the invention, Figure 1 illustrates an exemplary embodiment of an arrangement for carrying out the method according to the invention, in the form of a block diagram,
Figure 2 shows an exemplary embodiment of a filter for filtering the digital input variables,
Figure 3 shows the characteristic and structure of the filter according to Figure 2,

Figure 4 illustrates an exemplary embodiment of an interpolation filter, and
Figure 5 shows the characteristic and structure of the filter according to Figure 4.

As may be seen from Figure 1, there is present at an input 1 of an arrangement for carrying out the method according to the invention an analog input signal x(t) which is converted in an analog-to-digital converter 2 into a digital input signal x(k). This digital input signal x(k) traverses a signal encoder 3 formed by a differentiator, resulting at the output of the signal encoder 3 in a pulse train xd(k) which has been produced by differentiating the digital input signal x(k). A transmission device 4 transmits the pulse train xd(k) via a transmission channel 5 to a receiving device 6 which outputs the pulse train xd(k) on the output side.

The arrangement illustrated in Figure 1 includes a further receiving device 7 which is connected with its input 8 to a further input 9 of the arrangement in a way which was described in conjunction with the receiving device 6 with reference to the input 8. The dotted illustration is intended to include an analog-to-digital converter corresponding to the analog-to-digital converter 2, a signal encoder corresponding to the signal encoder 3, a transmitting device corresponding to the transmitting device 4, and a transmission channel corresponding to the transmission channel 5. A pulse train yd(k) obtained in accordance with the pulse train xd(k) of the signal y(t) is then produced at the output of the further receiving device 7.

In addition to the receiving device 7, it is also possible for further additional receiving devices to have additional pulse trains applied to them in the same way.

On the output side, a signal decoder 10, which includes a resampling device 11 on the input side, is connected to the receiving devices 6 and 7. This resampling device 11 can be designed and operated as illustrated in detail in US patent 5,075,880, particularly in Figure 5, and described in conjunction therewith. Thus, in the resampling device 11 the digital input signals xd(k) and yd(k) are respectively sampled per se with the aid of a common postprocessing clock of the resampling device, and digital auxiliary signals xd(nk+j) and yd(nk+j) are formed in the process by the insertion of zero values. In this case, the resampling device 11 is designed with regard to its postprocessing clock such that the latter is at least twice as fast as the fastest operating clock during the formation of the digital input signals x(k). For example, if the sampling frequencies for obtaining the digital input signals x(k) are between approximately 1 and 40 kHz, a frequency range of between 10 and 500 kHz comes into consideration for the postprocessing clock; approximately 200 kHz may be recommended.

The digital auxiliary signals xd(nk+j) and yd(nk+j) with the comparatively high postprocessing clock are fed in each case to an interpolation filter 12 and 13, respectively, which is an integrator in each case in the exemplary embodiment illustrated. The integrators are used in each case because differentiators have been used as signal encoders 3. A transmission characteristic with the value 1 thereby results with regard to the mode of operation of the signal encoder 3 and of the integrator 12 of the signal decoder 10.

Other interpolation filters also basically come into consideration, for example Lagrange interpolators or Spline interpolators.

The pulse trains x(nk+j) and y(nk+j) formed at the output of the integrators 12 and 13 are synchronized and are respectively fed to an antialiasing filter 14 and 15, by means of which filters the pulse trains are limited to the bandwidth required for processing in an evaluation device (not illustrated). The result is the reduction of digital output signals x(m) at the output of one antialiasing filter 14, and y(m) at the output of the other antialiasing filter 15. These digital output signals x(m) and y(m) can now be reduced in a known way to a sampling rate which is suitable for an evaluation device (not illustrated). This sampling rate must be produced by means of an integral devisor from the sampling rate of the resampling device 11. For the assumed frequencies, reasonable values here are between 0.6 and 10 kHz for applications in the monitoring of electric power supply systems.

If x(t) and y(t) are pure sinusoidal or cosinusoidal signals, it is then possible to dispense with the signal encoder 3 in each case. This also holds in the case of signals which are not pure sinusoidal or cosinusoidal ones whenever x(t) and y(t) are output variables of Rogovsky transducers because these output variables correspond to the differential quotient of the transducer input variables.

Illustrated in Figure 2 is an exemplary embodiment for a signal encoder 3 in accordance with Figure 1, which is designed as an FIR filter acting as a differentiator. Here, A denotes the input of the signal encoder, and B denotes the output. The digital input signal x(k) is used to form

the pulse train xd(k). The coefficients a_0, a_1 and b_1 of the signal coder 3 are dimensioned as follows:

Coefficient	Value
a0	0.66666666666667
a1	-0.66666666666667
b1	0.83333333333333

In the top illustration of Figure 3, the amplitude characteristic is illustrated plotted against the frequency of the signal encoder according to Figure 2, while in the bottom illustration of Figure 3 the phase characteristic is reproduced plotted against the frequency of such a filter.

The interpolation device 12 illustrated in Figure 4, or the interpolation device 13 in accordance with Figure 1 shows an FIR filter as integrator having coefficients a_0, a_1, b_1 dimensioned in a way which may be gathered from the following table. C denotes the input of this FIR filter, and D denotes its output.

Coefficient	Value
a0	1.50000000000000
a1	1.25000000000000
b1	-1

In the top illustration of Figure 5, the amplitude characteristic is shown plotted against the frequency of the filter according to Figure 4, and in the bottom illustration of Figure 5 the phase characteristic is shown plotted against the frequency of such a filter. It may be seen that the frequency characteristics of the filters according to Figures 2 and 4 are inverse relative to one another, and this leads to the targeted transmission function having the value 1.

Patent claims

1. A method for synchronizing a plurality of digital input signals ((x(k)), which are formed by sampling with the aid of a dedicated operating clock in each case, characterized in that

- digital auxiliary signals (xd(nk+j), yd(nk+j)) are formed by sampling the digital input signals (x(k)) with the aid of a common postprocessing clock,
- use being made of a postprocessing clock which is at least twice as fast as the fastest operating clock, and
- synchronized digital output signals (x(m), y(m)) which correspond to the digital input signals (x(k)) are formed by means of interpolating each digital auxiliary signal (xd(nk+j), yd(nk+j)).

2. The method as claimed in claim 1, characterized in that

- before being sampled with the aid of the common postprocessing clock, the digital input signals (x(k)) are filtered with the aid of a filter (3) having a characteristic which is the inverse of the characteristic of an interpolation filter (12, 13) used for the interpolation.

3. The method as claimed in claim 1 or 2, characterized in that

- filtering with the aid of an antialiasing filter (14, 15) is undertaken directly after the interpolation.

4. The method as claimed in one of the preceding claims, characterized in that

- the digital input signals are obtained from secondary variables, sampled with the aid in each case of a dedicated operating clock, of measuring.

transducers in an electric power supply system.

5. The method as claimed in claim 4, characterized in that

- in the case of digital input signals formed from secondary variables of Rogovsky measuring transducers the digital auxiliary signals are formed directly from these input signals, and
- an integrator is used for the interpolation.

Abstract

Method for synchronizing a plurality of digital input signals

The invention relates to a method for synchronizing a plurality of digital input signals which are formed by sampling with the aid of a dedicated operating clock in each case.

In order to be able to carry out such a method reliably with a relatively low outlay, according to the invention digital auxiliary signals (xd(nk+j), (yd(nk+j)) are formed by sampling the digital input signals (x(k)) with the aid of a common postprocessing clock, use being made of a postprocessing clock which is at least twice as fast as the fastest operating clock; synchronized digital output signals (x(m), y(m)) which correspond to the digital input signals (x(k)) are formed by means of interpolating each digital auxiliary signal (xd(nk+j), yd(nk+j)).

Figure 1

PCT WELTORGANISATION FÜR GEISTIGES EIGENTUM
Internationales Büro
INTERNATIONALE ANMELDUNG VERÖFFENTLICHT NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT)

(51) Internationale Patentklassifikation 7 : G06F 17/17

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(30) Prioritätsdaten:
198 60 720.2 23. Dezember 1998 (23.12.98) DE

(71) Anmelder *(für alle Bestimmungsstaaten ausser US)*: SIEMENS AKTIENGESELLSCHAFT [DE/DE]; Wittelsbacherplatz 2, D–80333 München (DE).

(72) Erfinder; und
(75) Erfinder/Anmelder *(nur für US)*: JURISCH, Andreas [DE/DE]; Eichenweg 11, D–16727 Schwante (DE).

(74) Gemeinsamer Vertreter: SIEMENS AKTIENGESELLSCHAFT; Postfach 22 16 34, D–80506 München (DE).

(81) Bestimmungsstaaten: CN, IN, US, europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

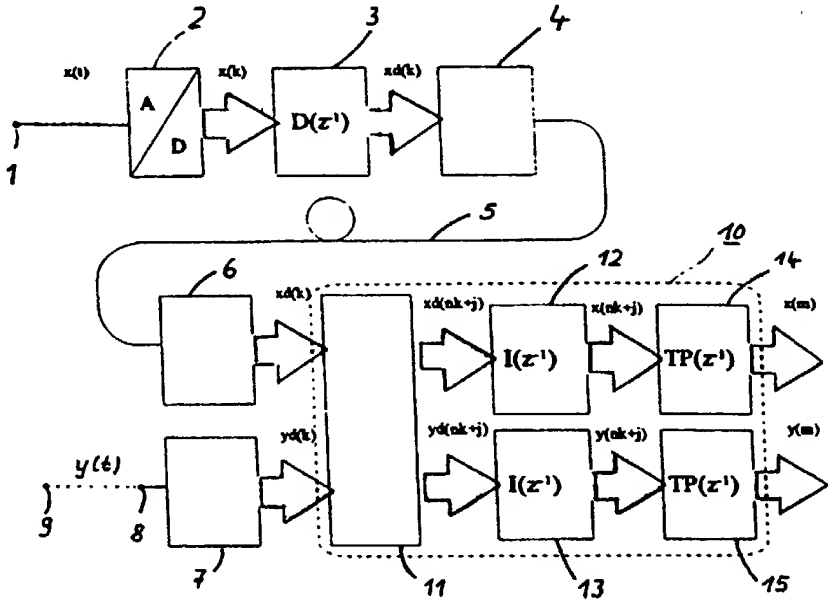
Veröffentlicht
Mit internationalem Recherchenbericht.

(54) Title: METHOD FOR SYNCHRONIZING SEVERAL DIGITAL INPUT SIGNALS

(54) Bezeichnung: VERFAHREN ZUM SYNCHRONISIEREN VON MEHREREN DIGITALEN EINGANGSSIGNALEN

(57) Abstract

The invention relates to a method for synchronizing several digital input signals that are formed by scanning with their own working clock pulse. According to the invention, in order to implement said method in a reliable manner and with relatively little complication, auxiliary digital signals (xd(nk+j), yd(nk+j)) are formed by scanning the digital input signals (x(k)) using a common postprocessing clock pulse that is at least twice as fast as the fastest working clock pulse. Synchronized output signals (x(m), y(m)) corresponding to the digital input signals (x(k)) are formed by interpolating each auxiliary digital signal (xd(nk+j), yd(nk+j)).



(57) Zusammenfassung

Die Erfindung bezieht sich auf ein Verfahren zum Synchronisieren von mehreren digitalen Eingangssignalen, die durch Abtasten mit jeweils einem eigenen Arbeitstakt gebildet sind. Um ein solches Verfahren zuverlässig mit relativ geringem Aufwand durchführen zu können, werden erfindungsgemäß durch Abtasten der digitalen Eingangssignale (x(k)) mit einem gemeinsamen Nacharbeitungstakt digitale Hilfssignale (xd(nk+j), yd(nk+j)) gebildet, wobei ein Nacharbeitungstakt verwendet wird, der mindestens doppelt so schnell wie der schnellste Arbeitstakt ist; mittels Interpolieren jedes digitalen Hilfssignals (xd(nk+j), yd(nk+j)) werden synchronisierte digitale Ausgangssignale (x(m), y(m)) gebildet, die den digitalen Eingangssignalen (x(k)) entsprechen.

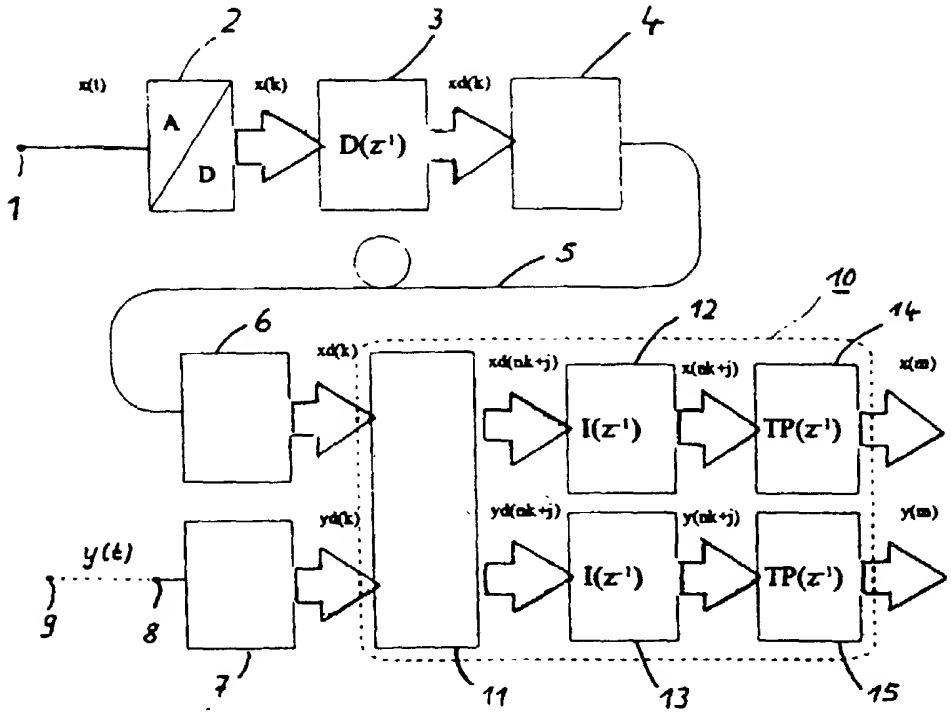

2
3
4
x(t)
x(k)
xd(k)
A
D
D(z⁻¹)
1
5
10
12
14
6
xd(k)
xd(nk+j)
x(nk+j)
x(m)
I(z⁻¹)
TP(z⁻¹)
yd(k)
yd(nk+j)
y(nk+j)
y(m)
y(t)
I(z⁻¹)
TP(z⁻¹)
9
8
7
11
13
15

Fig. 1

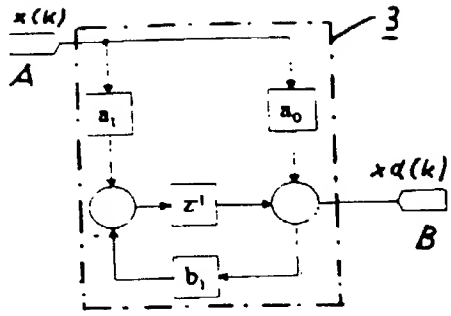

x(k)
A
3
a1
a0
xq(k)
B
z-1
b1

Fig.2

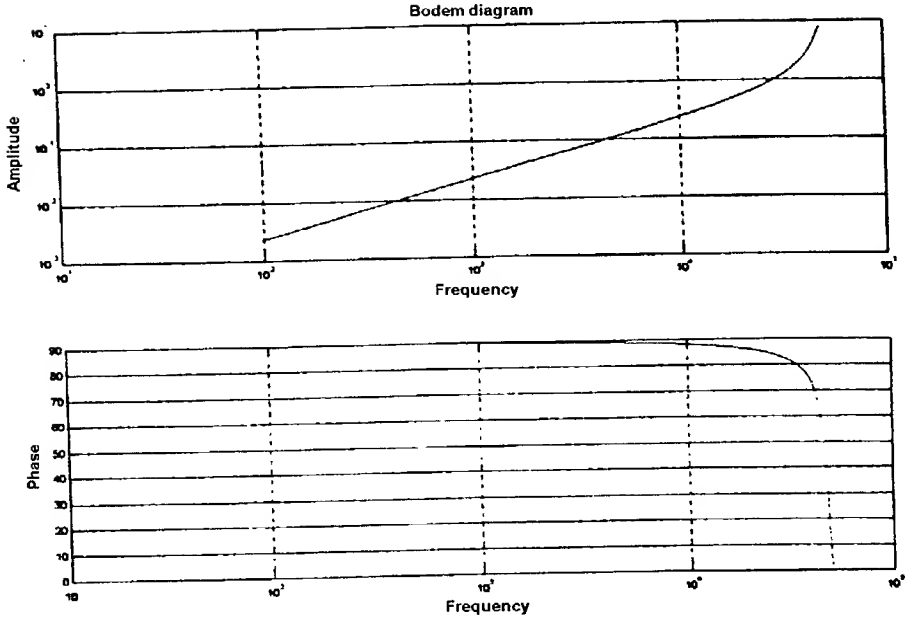

Bodem diagram
Amplitude
Frequency
Phase
Frequency

Fig. 3

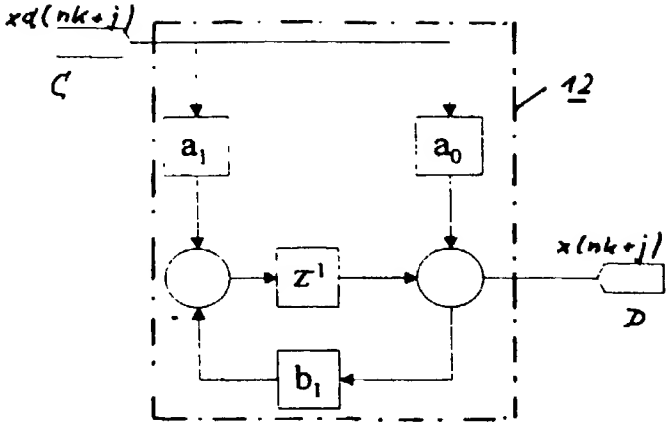

xq(nk+j)
C
12
a1
a0
z-1
x(nk+j)
D
b1

Fig. 4

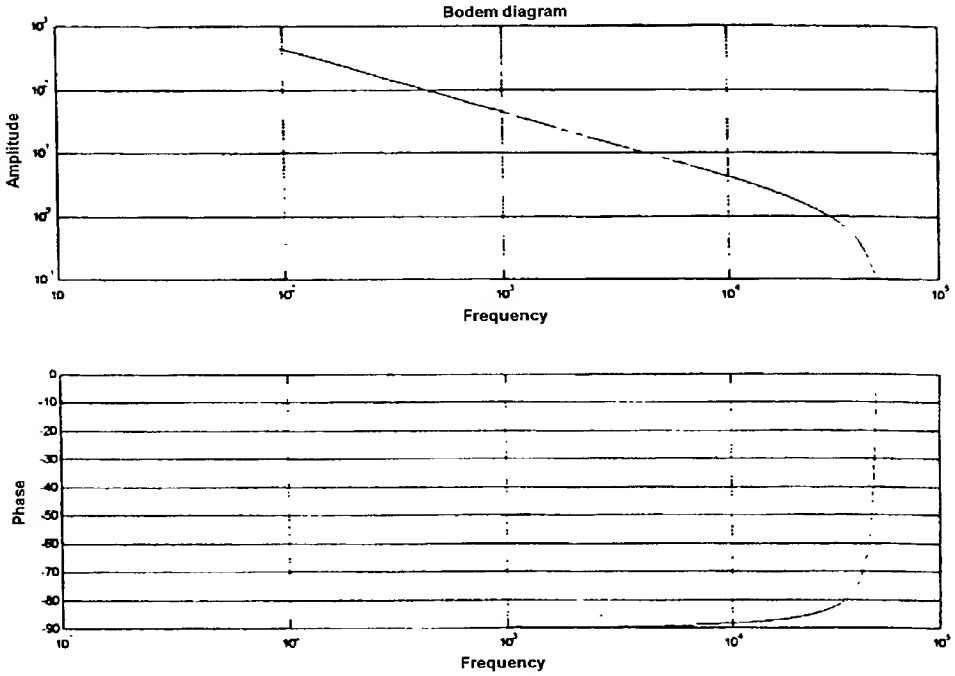

Bodem diagram
Amplitude
Frequency
Phase
Frequency

Fig. 5

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

VERFAHREN ZUM SYNCHRONISIEREN VON MEHREREN DIGITALEN EINGANGSSIGNALEN

deren Beschreibung

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 30.11.1999 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE99/03881
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR SYNCHRONIZING SEVERAL DIGITAL INPUT SIGNALS

the specification of which

(check one)
☐ is attached hereto.
☒ was filed on 30.11.1999 as
PCT international application
PCT Application No. PCT/DE99/03881
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

IDNR: 2590 / V: 99-1.00 / B:Val

German Language Declaration

Prior foreign appplications Priorität beansprucht			Priority Claimed	
19860720.2 (Number) (Nummer)	DE (Country) (Land)	23.12.1998 (Day Month Year Filed) (Tag Monat Jahr eingereicht)	☒ Yes Ja	☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes Ja	☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes Ja	☐ No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE99/03881 (Application Serial No.) (Anmeldeseriennummer)	30.11.1999 (Filing Date D, M, Y) (Anmeldedatum T, M, J)	_____ (Status) (patentiert, anhängig, aufgegeben)	pending (Status) (patented, pending, abandoned)
_____ (Application Serial No) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M, J)	_____ (Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent- und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

And I hereby appoint

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Telefongespräche bitte richten an: *(Name und Telefonnummer)*

Direct Telephone Calls to: *(name and telephone number)*

Ext. _____

Postanschrift:

Send Correspondence to:

MORRISON AND FOERSTER LLP
2000 PENNSYLVANIA AVE, NW 20006-1888 WASHINGTON, DC
Telephone: +1 202 887 1500 and Facsimile +1 202 887 0763
or
Customer No. 25227

Voller Name des einzigen oder ursprünglichen Erfinders:	Full name of sole or first inventor:
Dr. ANDREAS JURISCH	Dr. ANDREAS JURISCH
Unterschrift des Erfinders Datum: Andreas Jurisch 8.6.2001	Inventor's signature Date: Andreas Jurisch 06-08-2001
Wohnsitz: SCHWANTE, DEUTSCHLAND (DE)	Residence: SCHWANTE, GERMANY
Staatsangehörigkeit: DEUTSCH	Citizenship: GERMAN
Postanschrift: EICHENWEG 11 16727 SCHWANTE DEUTSCHLAND	Post Office Addess: EICHENWEG 11 16727 SCHWANTE GERMANY
Voller Name des zweiten Miterfinders (falls zutreffend).	Full name of second joint inventor, if any:
Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz ,	Residence ,
Staatsangehorigkeit	Citizenship
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(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).